Problem Statement

Define, Design, Develop and Characterize an Open-Loop Stereo Class-D Amplifier using the EPC GaN FET Technology and Devices for the purpose of providing an entry-level evaluation for the mid- to high-end Consumer and Pro-Sumer Amplifier market segment. Assess the IM/TIM implications of Open-Loop vs. Closed-Loop designs of the same topology.

Task Definition

Choose a known, low-risk Open-Loop Class-D Amplifier approach that is presently used in the Consumer and Pro-Sumer applications to characterize and validate the use of the EPC GaN FET devices in a target Stereo Amplifier Market Application. Integrate the necessary DSP for Audio Processing and for Audio Performance optimization of the Open-Loop architecture.

As a proof-of-concept for this market sub-segment, the amplifier platform design will be a two-channel, stand-alone design, with evident support for scalability and expandability. This target platform approach is also readily modified to a wide variety of cost-effective DSP Controllers, which support the proposed design architecture and topology.

The initial design will be a Bridge-Tied-Load (BTL) design, composed of four ground-referenced Half-Bridge Output Stages. This architecture and topology is the most scalable, and also demonstrates the target application requirements. In addition, it allows scalability to the power levels required for the broader target market with lower power supply voltages (< +/- 32VDC).

Planned Approach

For the purposes of comparison, the Open-Loop Class-D Amplifier will use exactly the same architectural and topological approach as the Closed-Loop EPC CLAM Module design. This will allow for comparisons using exactly the same end-to-end, “apples-to-apples” implementation so there is no room for concern that any difference in audio signal path might be the contributing factor for any measurement differences. Below is a photo of the Open-Loop Class-D Amplifier PCBA.

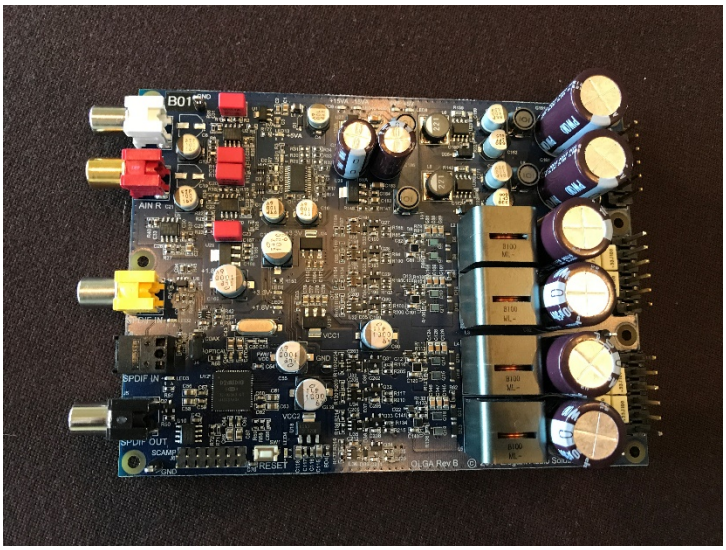

Figure 1: EPC eGaN FET Open-Loop Class-D Amplifier PCBA

Definition & Design

Choose an existing and proven Open-Loop Class-D amplifier architecture, and define and design a high-performance Stereo Amplifier with the following target specifications. Features, functions and architectural topology should be the same as that of the EPC CLAM Module.

Power Output	200Wrms into an 8-ohm load 400Wrms into a 4-ohm load
THD+N (open loop)	< 0.1% into an 8-ohm load, 1kHz < 0.2% into a 4-ohm load, 1kHz
SNR	> 110dB
Frequency Response	20Hz to 20kHz, +/- 0.5dB, 6-ohm
Switching Frequency	384kHz
Efficiency	> 93%
Power Supply Voltage	< +/- 32VDC for 2x BTL and Ground-Referenced Output

The chosen platform provides the following interfaces which support the application and evaluation requirements for the target market.

Input/Source	
Analog	Single-ended RCA Phono x 2, Unbalanced, $2V_{rms}$
Digital	Optical TOSLINK S/PDIF Digital Coaxial S/PDIF Digital
Power Supply	
Input	6-pin JST 0.156” Header (+HV, -HV, Ground)
Output	
Power	6-pin JST 0.156” Header x 2 (+L, G, -L, +R, G, -R)

For comparison purposes, the Closed-Loop EPC eGaN FET CLAM Module Evaluation Kit is shown below.

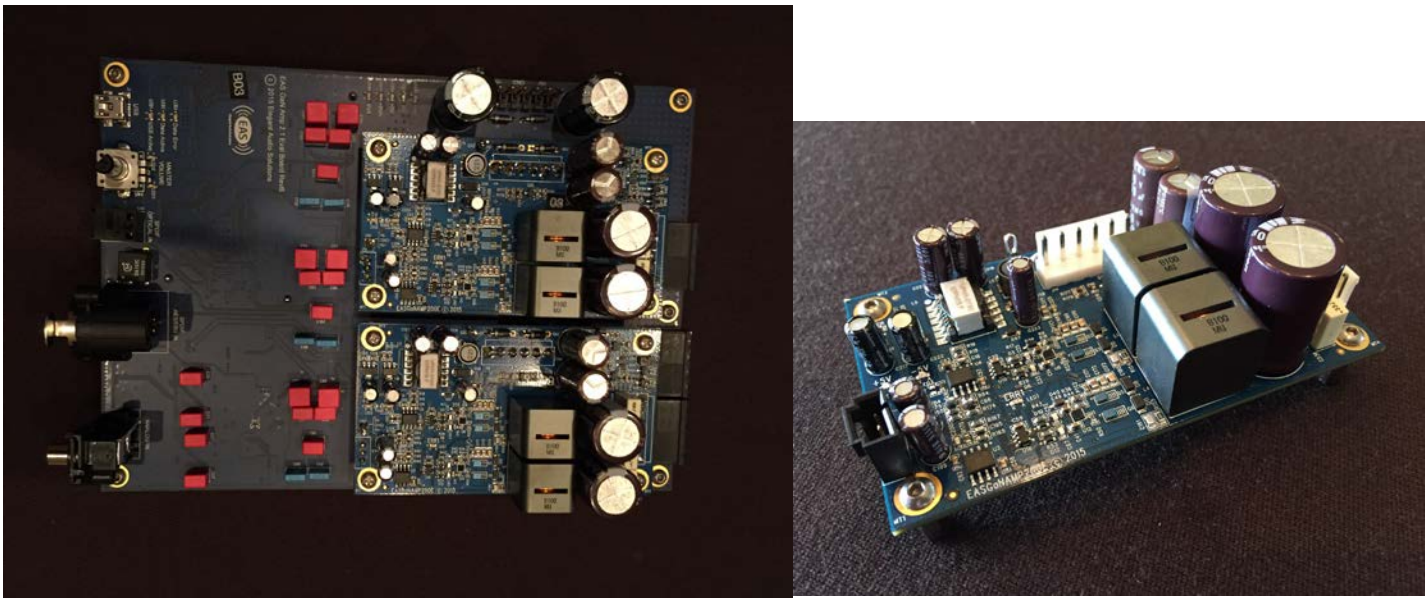

Figure 2: EPC eGaN FET CLAM Module Evaluation Kit

Prototype Test and Validation

The initial prototypes were tested and validated using industry-standard measurements, with recognized techniques and equipment. The Test Bench was set up with the following equipment for bring-up, test and validation:

Audio Precision AP2700 System Two Cascade w/AES-17 Filter
Topward 6603D Dual Output Power Supply

The standard set of industry performance and validation tests were run using this Test Bench. These tests were included for completeness, but were not necessarily considered to be the tests used for possible differentiation (although, as noted, they did provide the expected differentiation).

Performance Specification Testing
- Power Output (200W into 8 ohms)
- Power Output (400W into 4 ohms)
- Idle Dissipation
- Efficiency

Performance Characterization Testing
- THD+N vs. Power/Level
- THD+N vs. Frequency
- Frequency Response (8-ohm, 6-ohm, 4-ohm)
  - Limited by Audio Precision AES-17 Brick-Wall Filter
- Noise Floor (SNR)

Base Test Results and Characterization

To follow are the results of both the initial Characterization that was performed on the eGaN FET Class-D Amplifier platforms. Unless otherwise noted, the Characterization was performed under the Power Supply conditions that allow for the specified Target Market specification of 200W/8-ohms. This requirement resulted in Power Supply Voltage rails of +/-32VDC. This selected Power Supply definition provides up to 200W of clean power into 8 ohms, (as captured in Figure 1 below).

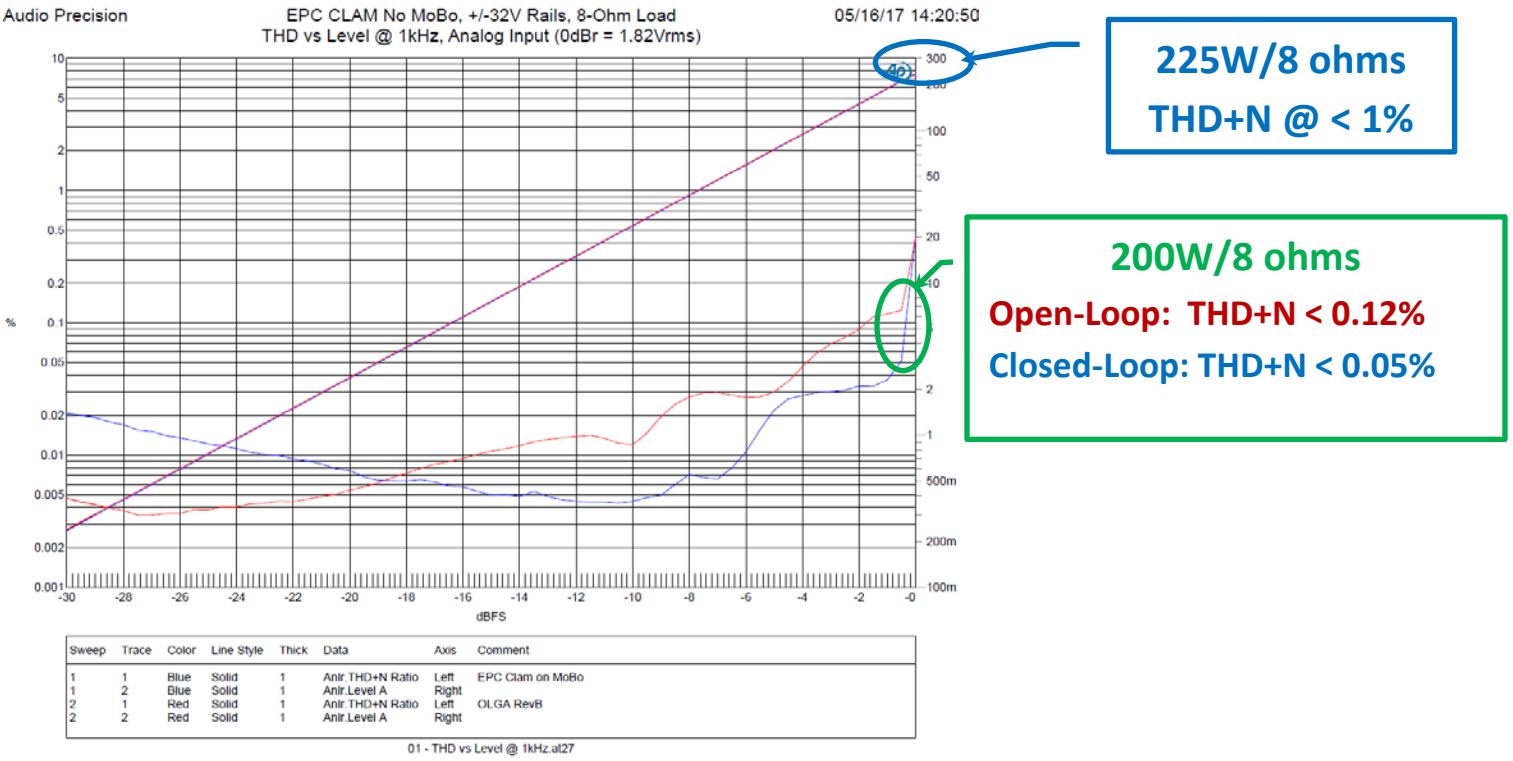

Figure 3: THD+N vs. Power into 8 Ohms @ +/-32VDC

From the THD+N vs. Level (Power) plot, it can be readily determined that the low signal-level THD performance for the Open-Loop Amplifier exceeds that of the Closed-Loop approach. This is mainly due to the increase Noise contribution of the Feedback, and can easily be understood by comparing this snapshot to the Noise Floor performance illustrated below in Figure 5.

As the audio signal level is increased, and hence the output power increased, the benefit of the Closed-Loop architecture is evident. However, the THD+N of the Open-Loop architecture compares very favorably, mainly due to the excellent switch characteristics of the eGaN FET in the Output Stage. By using an Open-Loop architecture with the ability to tightly control the Deadband timing, near Closed-Loop THD performance can be achieved.

This is readily perceived in the THD+N vs. Frequency plots below, as well. The increase in THD+N with the Open-Loop architecture, and at the lower frequencies in mainly due to the lack of Power Supply rejection, and the contribution to the system-level performance by the SMPS.

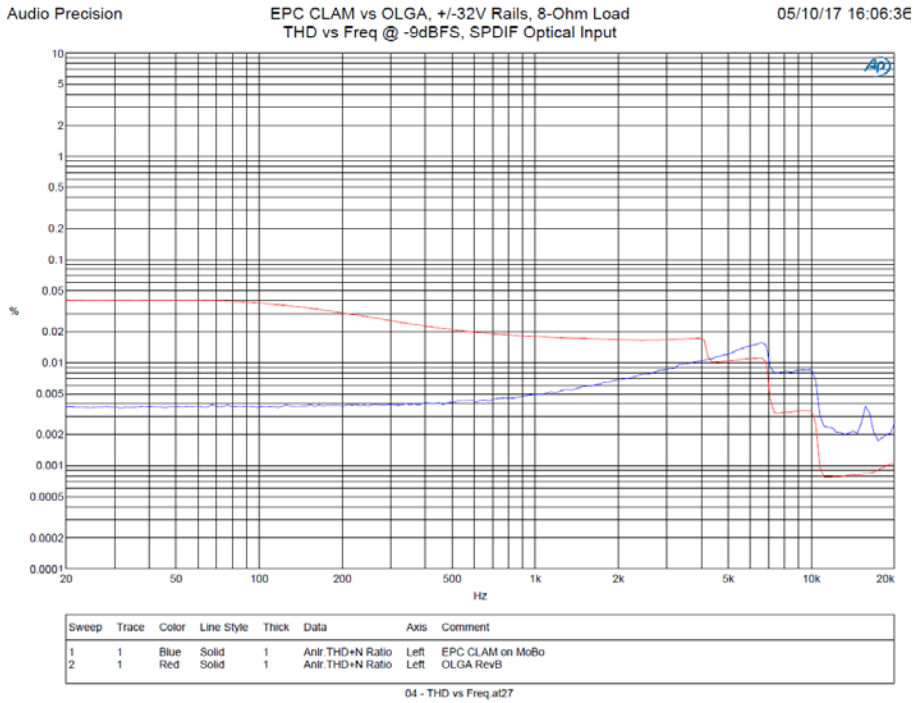

Figure 4: THD+N vs. Frequency

However, as with the THD+N vs. Level measurements, the Open-Loop architecture very quickly approaches the performance of the Closed-Loop architecture in the upper-mid-range.

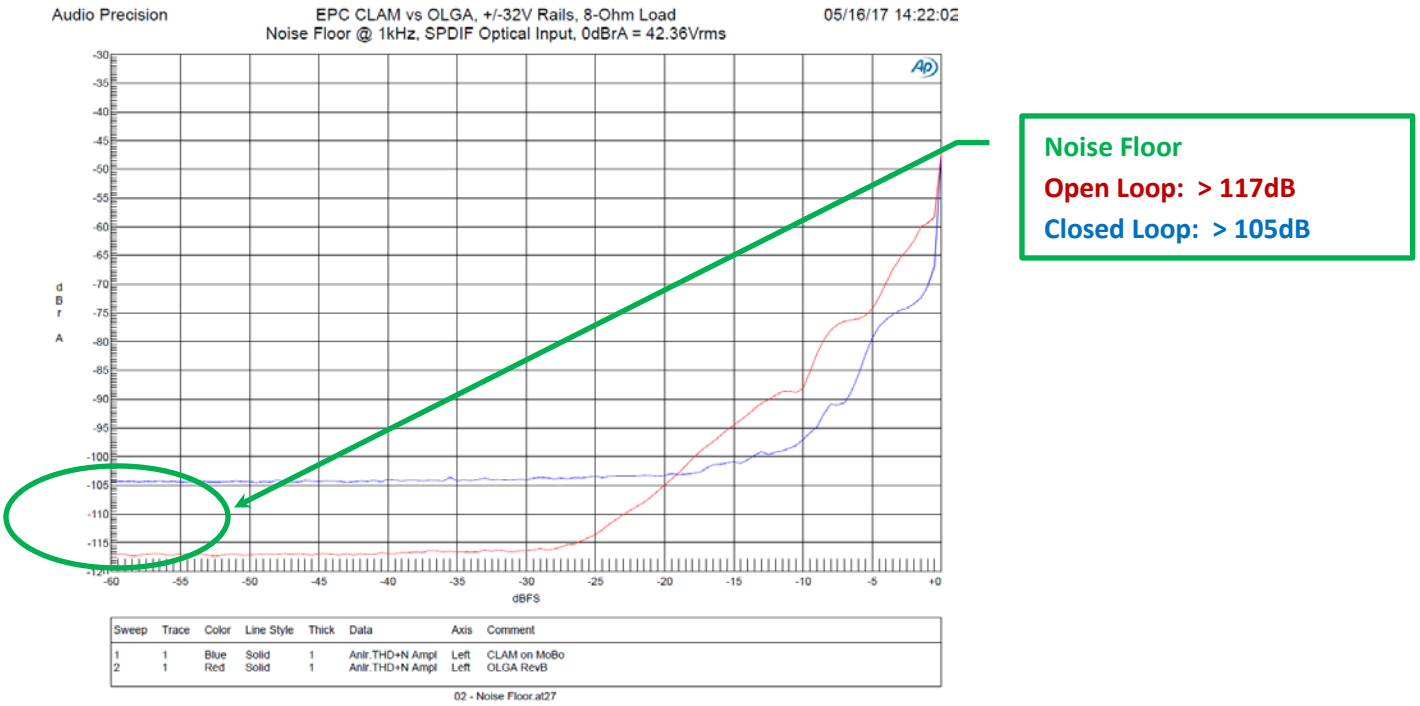

Figure 5: Noise Floor

As mentioned above, this huge (12dB) difference in Noise Floor ultimately affects the low-signal-level performance of all audio measurements. These measurements establish a "baseline" for the IM/TIM characterization that was the basis for this follow-on study.

IM/TIM Test Results and Characterization

To follow are the results from the IM/TIM Characterization comparison that was performed on the two eGaN FET Class-D Amplifier platforms. Unless otherwise noted, the Characterization was performed under the same Power Supply conditions that were referenced for the above characterization.

A wide range of IM/TIM Tests were performed to assure a full capture of the comparative performance between the two similar platforms: Open-Loop and Closed-Loop. The following Audio Precision Tests were performed:

DIM B Sweep
DIM 30 Sweep
DIM 100 Sweep
SMPTE Sweep
CCIF Sweep
SMPTE FFT 60Hz 7kHz
SMPTE FFT 60Hz 6kHz
SMPTE FFT 60Hz 3kHz
CCIF FFT

It is important to use both the "Sweep" and the "FFT" measurements to capture a more accurate view of the IM/TIM performance, as using either one of these measurement techniques alone and provide deceiving results, or at best, misleading results.

The following discussion, which accompanies these measurement plots, attempts to correlate the two different measurement techniques, and describe how to extract the best overall picture of IM/TIM performance of these two platforms.

Rather than repeat the definitions and descriptions of these Tests here, the following Audio Precisions documents will accompany this report:

"2700 Series Instrument Specifications"
"DIM 30 and DIM 100 Measurements per IEC 60268-3 with AP2700"

Measured Performance Summary

Due to the proposal budget and timeframe (along with the anticipated time for the optimization described above), a target platform was chosen to assure a "first-time" success from a single platform development. This "first-time" success required that an architectural approach be chosen with a well-defined topology and a well-known level of risk. This platform choice ultimately restricted the way in which many of the desired assessments could be accomplished. It did, however, provide the desired "out-of-the-box" functionality for the basic performance assessment.

NOTE: It is important to understand that the "optimizations" that were attempted over the course of this initial effort are more preferably performed with the "open-loop" architecture, where the loop is "closed" only after the "optimization". Optimization of "open-loop" performance allows for much better visibility into the actual contributions of each component to the overall performance, where "closed-loop" optimization is often obscured by the feedback.

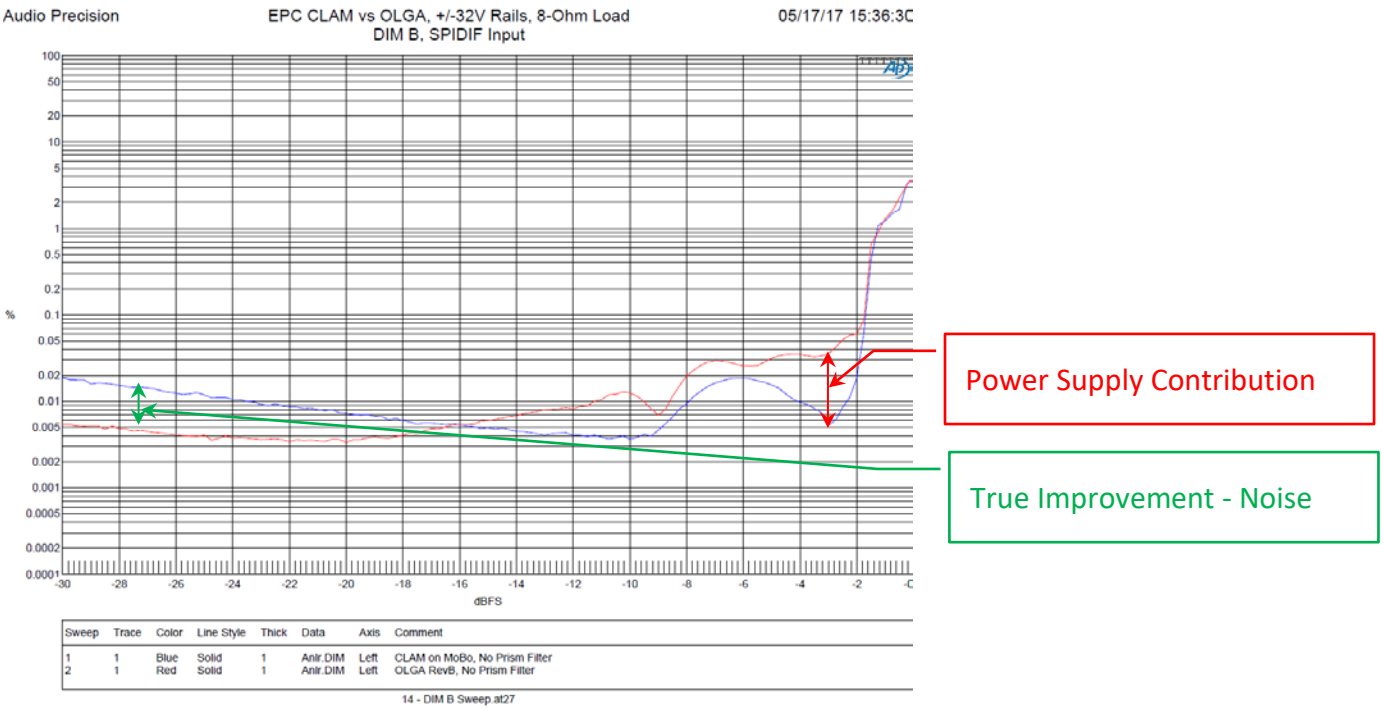

Figure 6: DIM B Comparison Plots (Open-Loop vs. Closed-Loop)

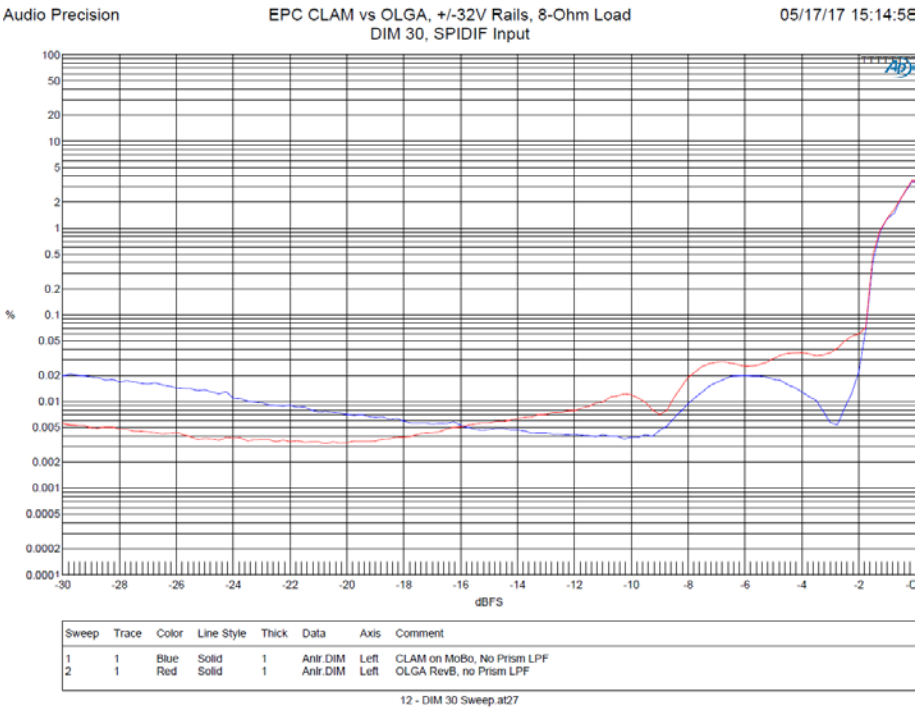

Figure 7: DIM 30 Comparison Plots (Open-Loop vs. Closed-Loop)

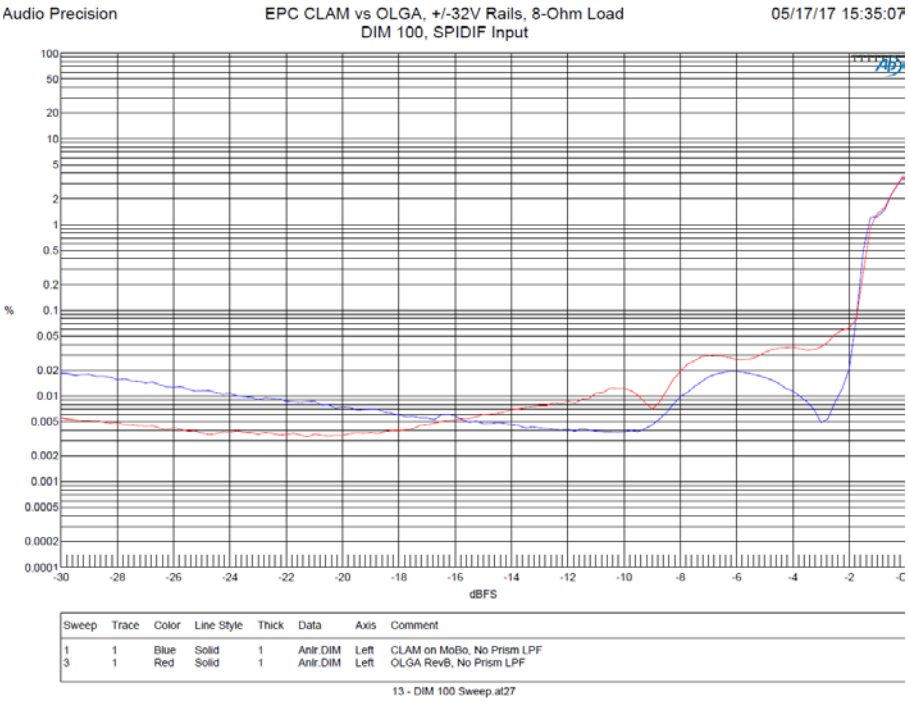

Figure 8: DIM 100 Comparison Plots (Open-Loop vs. Closed-Loop)

For the SMPTE and CCIF Sweeps, done vs. Frequency @ -9dBFS, the difference is still predominantly due to Power Supply coupling. This is further indicated by the relatively linear Distortion vs. Frequency capture.

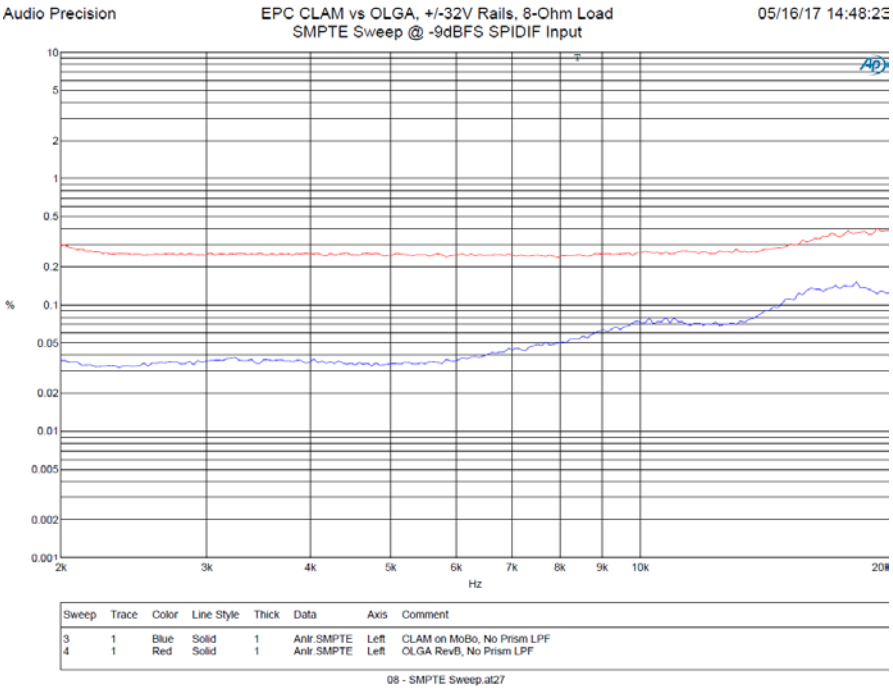

Figure 9: SMPTE [Sweep] FFT Comparison Plots (Open-Loop vs. Closed-Loop)

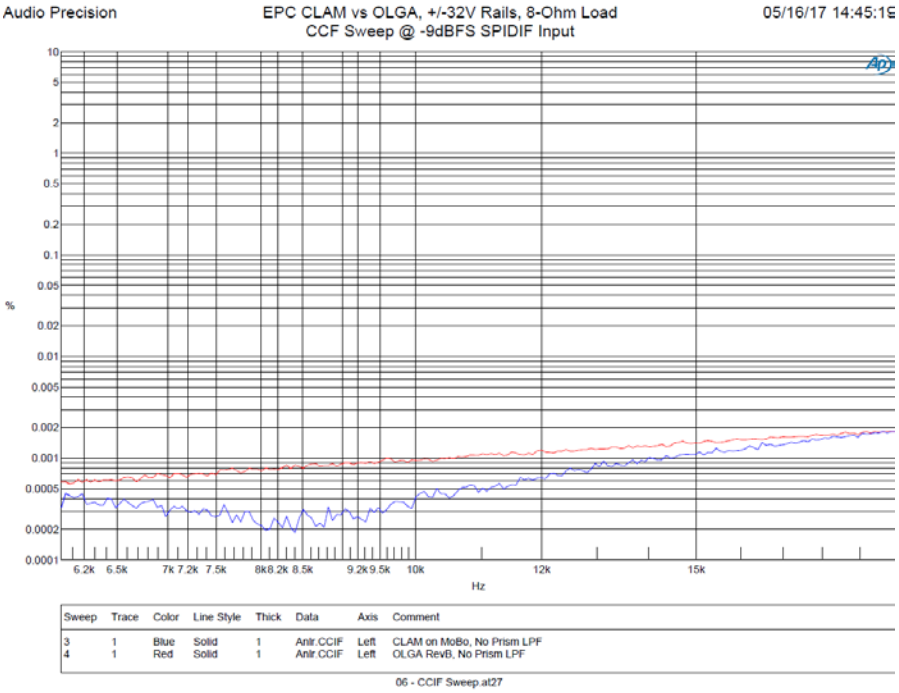

Figure 10: CCIF Sweep Comparison Plots (Open-Loop vs. Closed-Loop)

The FFT plots provide an excellent picture of the true contributions of both the Power Supply-induced Distortion and the actual improvement in IM/TIM. Note the two different components of the Power Supply-induced Distortion. The Closed-Loop components tend to be more composed of “Even” harmonics, while the Open-Loop components tend toward the “Odd” harmonics. This is due to the

intermodulation on the Power Supply itself. From the overall plot, the improved IM/TIM of the Open-Loop topology is evident.

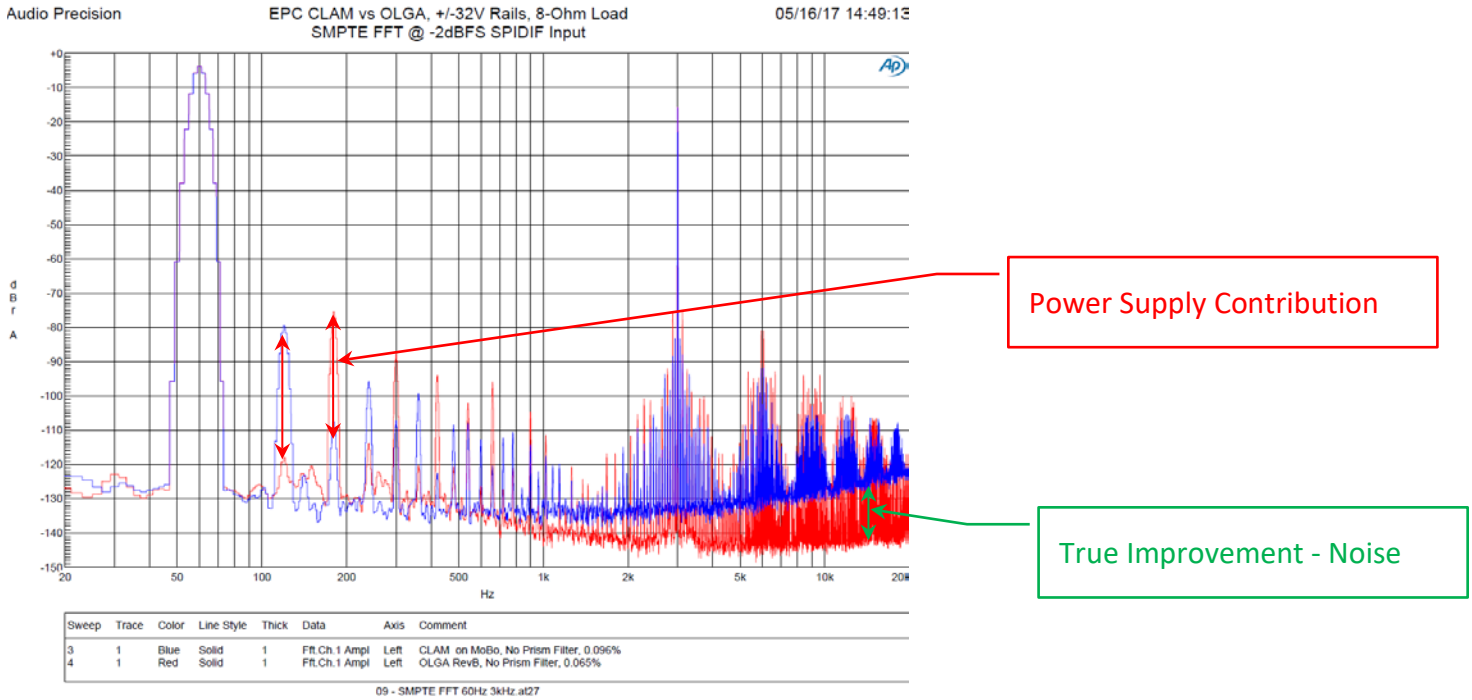

Figure 11: SMPTE [60Hz:3kHz] FFT Comparison Plots (Open-Loop vs. Closed-Loop)

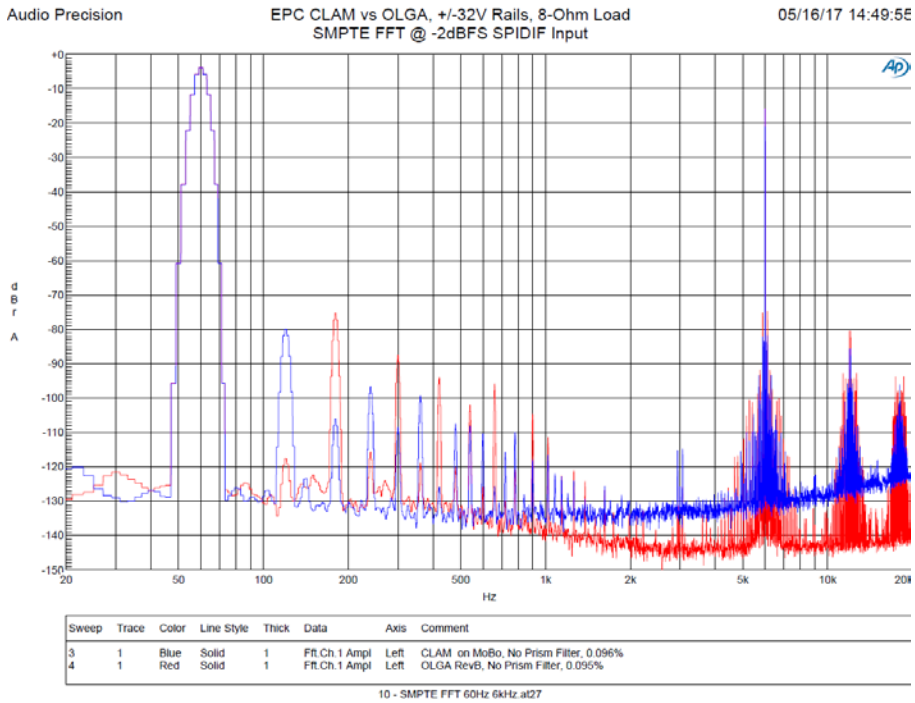

Figure 12: SMPTE [60Hz:6kHz] FFT Comparison Plots (Open-Loop vs. Closed-Loop)

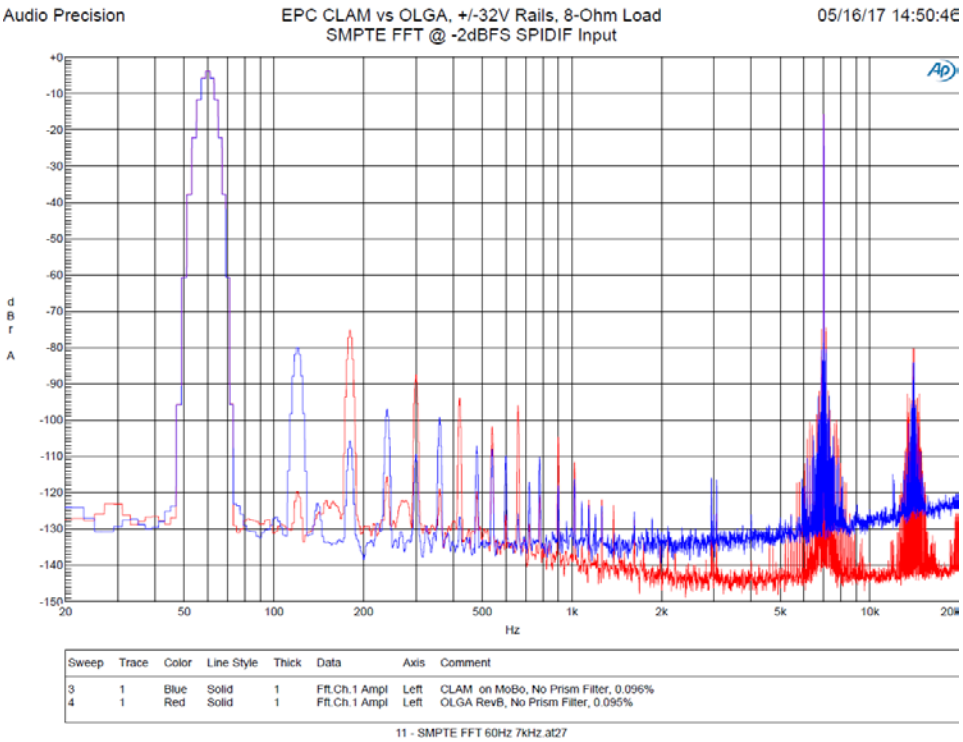

Figure 13: SMPTE [60Hz:7kHz] FFT Comparison Plots (Open-Loop vs. Closed-Loop)

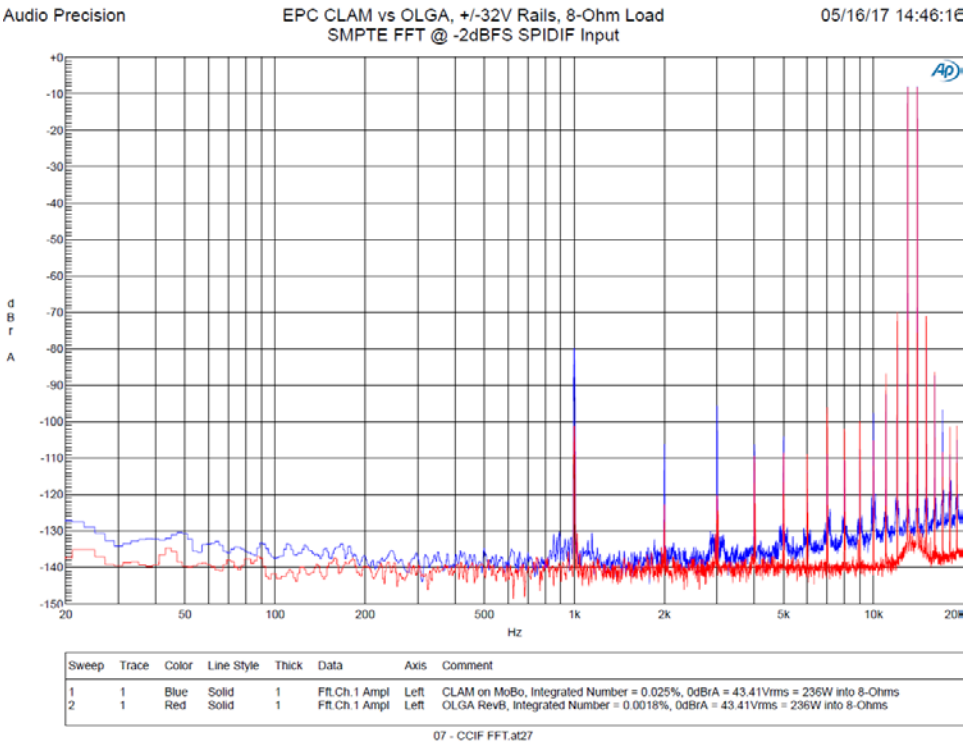

Figure 14: CCIF FFT Comparison Plots (Open-Loop vs. Closed-Loop)

Conclusions

The conclusions from this initial development effort are readily apparent from the above discussion. There were no real surprises in the data that was gathered or summarized. One thing that was very exciting and positive is that the performance of the Open-Loop platform is so good, in general (normal performance measurements: THD+N, Noise, Frequency Response, etc.), as compared to an almost identical Closed-Loop platform. In summary, the results can be captured as:

1) Industry-Standard Characterization results are at least as good, if not better than those of comparable Closed-Loop platform designs
2) The use of equally good Open-Loop topologies allows for the elimination of complexities associated with the Closed-Loop design counterpart
3) The Open-Loop topology allows for both “static” and “real-time” optimization of audio performance vs. EMI/EMC profile vs. thermal performance
4) The realized reduction in IM/TIM increases the sonic performance, without the associated loss in measured performance
5) For the Open-Loop topology, the Power Supply becomes an even more important component in the overall audio system solution
6) The Noise performance of the Open-Loop platform is near the theoretical maximum, opening the door to use in higher-efficiency, higher power Professional Audio platforms
7) The simplicity of the design will also allow for the integration of higher-power, multi-die, single package audio amplifiers for a broader market penetration